REMARKS

I. <u>Preliminary Remarks</u>

Independent Claims 1 and 21 have been amended. Claim 22 has been canceled. New claims 36-38 have been added. Claims 1-21 and 23-38 are now pending. Reconsideration and allowance of all of the claims in view of the above amendments and the following remarks are respectfully requested.

II. 102(b) and 103(a) References Cited

One aspect of the invention is to use a clock within a digital signal processor (DSP) to provide the operational clock frequencies for a pulse width modulated power (PWM) supply and a PWM amplifier so that all of the clock frequencies are synchronized for the DSP, the PWM supply, and the PWM amplifier. In this regard, independent claim 17, recited, in part, that "wherein said digital signal processor and said pulse width modulated power supply and said pulse width modulated power amplifier use said clock in said digital signal processor for its operational clock frequency."

The office action rejected claim 17 under 35 U.S.C. 103(a) as being obvious over Adrian et al. (U.S. Patent No. 5,617,058) in view of Ferland et al. (U.S. Patent No. 5,883,523). According to the office action, "[a]lthough, Adrian does not disclose the crystal timing reference being located internal to the digital signal processor (50), it does not make a difference if the crystal timing reference where internal or external to the DSP because it will have the same functionality regardless."

Applicant respectfully traverses the rejection. In Adrian and Ferland, a separate and distinct clock or timing device is used to provide a timing reference. For example, Adrian uses a crystal timing reference 53 (See Figure 10), and Ferland uses a clock source 28 (See Figure 1). In claim 17 of the present application, however, a clock within the DSP is used to provide the operational clock frequencies for the PWM supply, the PWM amplifier, and DSP so that all of the clock frequencies are synchronized without the need for a separate clock as taught by Adrian and Ferland. In other words, in the claimed invention, synchronized operational clock frequencies are provided to the PWM supply, the PWM amplifier, and DSP by using the clock in the DSP rather than using a separate clock.

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Omission of an element with retention of the element's function is an indicia of

unobviousness. See MPEP 2144.04 II. B., citing In re Edge, 359 F.2d 896, 149 USPQ (CCP)

1966). Accordingly, Applicant respectfully submits that Adrian and Ferland do not obviate the

claimed invention as recited in claim 17. In this regard, independent claims 1 and 21 have been

amended to recite, in part, that a clock within the DSP is used by a PWM power processing

device for synchronizing the operational clock frequencies. In addition, a new independent

claim 36 recites, in part, that PWM supply and amplifier use a clock in the DSP for their

respective operational clock frequency. As such, Applicant respectfully submits that the

independent clams 1, 17, 21, and 36, and their respective dependent claims are allowable over

the references cited by the office action.

IV Conclusion

In view of the foregoing, it is respectfully submitted that the claims in the application

patentably distinguish over the cited and applied references and are in condition for allowance.

Reexamination and reconsideration of the application, as amended, are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance,

the Examiner is respectfully requested to call Applicant's undersigned representative at (213)

689-5176 to discuss the steps necessary for placing the application in condition for allowance.

The Commissioner is hereby authorized to charge any additional fees which may be

required, or credit any overpayment to Deposit Account No. 07-1853. Should such additional

fees be associated with an extension of time, applicant respectfully requests that this paper be

considered a petition therefor.

Respectfully submitted,

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